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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,563	03/17/2004	Hong Yu Yu	NUS03-001	3494

7590 11/23/2005

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EXAMINER	
KIM, SU C	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,563	YU ET AL.	
	Examiner	Art Unit	
	Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-27 and 35-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-27 and 35-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/23/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment was received on 9/01/2005, and has been entered and made of record. Currently, claims 8-27 are pending and claims 35-52 are added.

Drawings

1. The correct or substitute specification was received on 9/01/2005. The Drawing is acceptable.

Specification

2. The correct or substitute specification was received on 9/01/2005. The Specification is acceptable.

Response to Arguments

3. Upon review of the reference of Matsuo (US Pub 2004/0183143), which was cited in the Office Action dated 5/27/2005 under 35 U.S.C 102 (b), as anticipating claims 8,16, 24, 26, & 27, the Examiner notes that the reference can still be interpreted as anticipating the claims, as currently amended.

Applicants contend that Matsuo (US Pub 2004/0183143) herein know as Matsuo fails to teach a CMOS gate electrodes by depositing and patterning a hafnium nitride metal layer as recited from claim 8.

In response to applicants' contention that Matsuo fails to teach CMOS gate electrodes by depositing and patterning a hafnium nitride metal layer as recited from

claim 8. Applicants are severely mistaken the teaching of Matsuo although the prior art does not use non inventive terms such as depositing and patterning a hafnium nitride layer. However, Matsuo clearly discloses hafnium nitride film is formed by CVD (CVD stands for Chemical vapor deposition) **(Paragraph [0015])** and pattern on N-type Misfet.

Therefore, the rejections under 35 U.S.C 102 of claims 8, 16, 24, 26, & 27 as being anticipated by Matsuo stand.

Applicant contend that The paper "Physical and Electrical Characteristics of HfnN Gate Electrode for Advanced MOS Devices", by authors H. Y. Yu, H. F. Lim, J. H. Chen, M. F. Li, Chunxiang Zhu, C. H. Tung, A. Y. Du, W. D. Wang, D. Z. Chi, and D. L. Kwong, is not believed to be a valid prior art reference under 35 USC 102.

In response to applicants' contention the paper "Physical and Electrical Characteristics of HfN Gate Electrode for Advanced MOS Devices", by authors H. Y. Yu, H. F. Lim, J. H. Chen, M. F. Li, Chunxiang Zhu, C. H. Tung, A. Y. Du, W. D. Wang, D. Z. Chi, and D. L. Kwong, is a valid prior art reference under 35 USC 102.

Due to date filed on The paper "Physical and Electrical Characteristics of HfnN Gate Electrode for Advanced MOS Devices", by authors H. Y. Yu, H. F. Lim, J. H. Chen, M. F. Li, Chunxiang Zhu, C. H. Tung, A. Y. Du, W. D. Wang, D. Z. Chi, and D. L. Kwong" the paper is earlier published date on April 2003, The paper clearly consider as 35

U.S.C 102 (a), but fail to teach all the limitation as claimed on claims 9 & 17. The paper is a valid prior art reference under 35 U.S.C 103(a). See MPEP706.02

35 U.S.C. 102 Conditions for patentability; novelty and loss of right to patent.

A person shall be entitled to a patent unless —

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or

4. MISFET and MOSFET are exchangeable on the prior art. MOSFET stands for Metal oxide semiconductor filed effect transistor, MISFET stands for metal insulator semiconductor because Matsuo teaches Silicon substrate **100** and complementary device Matsuo's MISFET is merely nothing more than applicant claimed MOSFET. Matsuo discloses CMISFET (Complementary metal insulated Field effect transistor with Silicon oxide film) is merely nothing but CMOS as claimed on Applicant's amendment.

5. Applicants' arguments filed on 9/01/2005 is have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8, 16, 24, 26 & 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuo (US 2004/0183143)

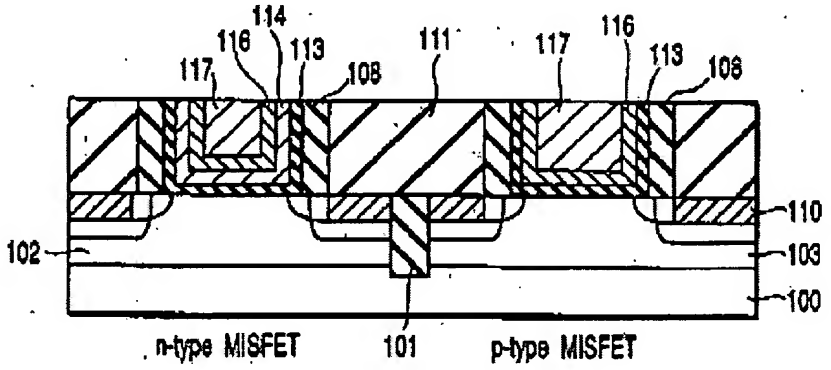

FIG. 3J
(PRIOR ART)

Matsuo discloses a method of fabricating semiconductor device as claimed. **See all the FIGS** where Matsuo teaches the following limitations

1. Pertaining to claim 8, discloses a method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer **113** on a substrate **100**;

depositing a hafnium nitride layer **114** overlying said dielectric layer **113**;

depositing a capping layer **116 & 117** overlying said hafnium nitride layer **114**;

patterning said hafnium nitride layer **114** and said capping layer **116 & 117** and said dielectric layer **113** to form CMOS gate and forming source and drain regions **109** within said substrate **100** adjacent to said CMOS gate electrode.

2. Pertaining to claim 16, A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer **113** on a substrate **100**;

depositing a first metal layer **114** overlying said dielectric layer **113**;

patterning said first metal layer **114** and said dielectric layer **113** to form CMOS gate electrode ; and

forming source and drain regions **109** within said substrate adjacent to said CMOS gate electrode.

3. Pertaining to claim 24, The method according to Claim 17 further comprising, depositing a second metal capping layer **116 & 117** overlying said first metal layer **114** prior to said patterning wherein said second metal is different from said first metal

(please note a first metal layer is hafnium nitride and a second metal is tantalum nitride).

4. Pertaining to claim 26, The method according to Claim 24 wherein said first metal layer comprises hafnium nitride **114** and wherein said second metal layer comprises tungsten or tantalum nitride **116**.

5. Pertaining to claim 27, The method according to Claim 24 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition **(Page 1 paragraph [0015] & [0019] Please note hafnium nitride & tantalum nitride are both metal having work function of 4.6eV or less is formed by CVD or Sputtering with a thickness of about 10 nm or less than 10nm, on the entire surface of the resultant).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9 & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo in view of Yu et al. (Electron Device Letters, IEEE Volume 24, Issue 4, April 2003 Page(s): 230 – 232).

Pertaining claims 9 & 17, Matsuo teaches the method according to claims 8 & 16, where said depositing of said hafnium nitride layer.

However, Matsuo does not disclose expressly deposing of hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously where said chamber contains said substrate and a hafnium target.

Yu discloses deposing of Hafnium nitride (HfN) layer comprise flowing Nitrogen and Argon atoms into a chamber simultaneously where said chamber contains said substrate and a hafnium target.

Matsuo and Yu are analogous art because they are from the same field of endeavor and a process of depositing HfN on the substrate.

At the tome of invention it would have been obvious to a person of ordinary skill in the art using a process to deposit HfN with flowing Nitrogen and Argon atoms into chamber because of utilizing for its material characterization (page 230 column 2 lines 11-12).

7. Claim 13 & 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo in view of Yu.

Matsuo does not discloses the method according to Claim 8 & 17 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one.

Yu discloses expressly the method according to Claim 8 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one **(Page 230 column 2 lines 15-17 & 29-32)**.

Matsuo and Yu are analogous art because they are from the same filed of endeavor and the name of a process of depositing HfN with flowing Nitrogen and Argon gases.

At the time of invention it would have been obvious to a person of ordinary skill in the art using the method according to Claim 8 & 17 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains

greater than or equal to one because HfN films show stoichiometric composition (Hf: N ~1:1).

8. Claims 14 & 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo in view of Yu.

Pirating claims 14 & 22 Matsuo discloses the method according to Claims 8 & 17.

However, Matsuo does not disclose expressly further comprising impurity doping into said hafnium nitride layer to tune the work function of said gate electrode.

Yu discloses expressly further comprising impurity doping into said hafnium nitride layer to tune the work function of said gate electrode (Page 230 column 2 lines 35-38, please note combining Yu's method of impurity doping into Matsuo's tuning the work function of gate electrode).

Matsuo and Yu are analogous art because they are from the same filed of endeavor and the name of a process of tuning the work function of gate electrode

At the time of invention it would have been obvious to a person of ordinary skill in the art combining the Yu's method of impurity doping into the Matsuo's methods of

fabrication semiconductor process because of oxidization and conversion into HfO_xN_y (Page column 2 lines 35-37).

Therefore, it would have been obvious to combine a Yu's method into Matsuo . methods for the benefit of newly crystalline plane by the HfO_xN_y to obtain the invention as specified in claim.

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Matsuo.

Pertaining to claim 25, The method according to Claim 24 wherein said first metal layer comprises tungsten or tantalum nitride and wherein said second metal layer comprises hafnium nitride.

Changes in sequence or process steps are merely nothing more than a prima facie obvious in the absence of new or unexpected results.

See Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is

prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie
obvious.).

10. Claims 10-12, 15, 18-20, & 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo in view of determining the optimum thickness, temperature as well as condition of delivery of the layers involved.

Pertaining to claim 10, Matsuo does not teaches the method according to claim 9 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

Pertaining to claim 11, Matsuo does not teaches the method according to Claim 8 wherein said dielectric layer comprises Hf02 and is deposited at 400°C using a MOCVD cluster tool.

Pertaining to claim 12, Matsuo does not teaches the method according to Claim 8 wherein said dielectric layer comprises Hf02 and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in N2 ambient.

Pertaining to claim 15, Matsuo does not teaches the method according to Claim 8 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

Pertaining to claim 18, Matsuo does not teaches the method according to claim 17 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

Pertaining to claim 19, Matsuo does not teaches the method according to Claim 16 wherein said dielectric layer comprises Hf02 and is deposited at 400°C using a MOCVD cluster tool.

Pertaining to claim 20, Matsuo does not teaches the method according to Claim 16 wherein said dielectric layer comprises Hf02 and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in N2 ambient.

Pertaining to claim 23, Matsuo does not teaches the method according to Claim 17 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers

involved. *See In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodru* ; 919 f 2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizake*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 35, 37, 40, 41, 42, & 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuo (US 2004/0183143)

11. Pertaining claim 35, Matsuo discloses a method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer **113** on a substrate **110**;

depositing a hafnium nitride layer **114** overlying said dielectric layer **113**;

depositing a titanium nitride or tungsten capping layer **116** overlying said hafnium nitride layer **114**;

patterning said hafnium nitride layer and said capping layer and said dielectric layer to form CMOS gate electrodes; and

forming source and drain regions **109** within said substrate adjacent to said CMOS gate electrodes **117**.

12. Pertaining claim 37, Matsuo discloses the method according to Claim 35 wherein said dielectric layer comprises HfO_2. **(Paragraph [0014] , Please note the dielectric materical can be Hafnium oxide (HfO_2)).**

13. Pertaining claim 40, Matsuo discloses a method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer **113** on a substrate **100**;

depositing a first metal layer **114** overlying said dielectric layer;
depositing a second metal capping layer **116** overlying said first metal layer **114**;

pattering said first metal layer **114**, said second metal capping layer **116**, and said dielectric layer **113** to form CMOS gate electrodes; and

forming source and drain regions **119** within said substrate adjacent to said CMOS gate electrodes **117**.

14. Pertaining claim 41 Matsuo discloses the method according to Claim 40 wherein said dielectric layer comprises HfO2 **(Paragraph [0014] , Please note the dielectric materical can be Hafnium oxide (HfO_2)).**

15. Pertaining claim 42, Matsuo discloses the method according to Claim 40 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition **(Paragraph [0015])**.

16. Pertaining claim 48, Matsuo discloses the method according to Claim 40 wherein said first metal layer comprises hafnium nitride **114** and wherein said second metal layer comprises tungsten or tantalum nitride **116**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36, 38, 39, 43, 44, 45, 47, 49, 50, 51 & 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo in view of Yu et al. (Electron Device Letters, IEEE Volume 24, Issue 4, April 2003 Page(s): 230 – 232).

17. Pertaining claim 36, Matsuo teaches the method according to claim 35, where said depositing of said hafnium nitride layer.

However, Matsuo does not disclose expressly deposing of hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously where said chamber contains said substrate and a hafnium target.

Yu discloses deposing of Hafnium nitride (HfN) layer comprise flowing Nitrogen and Argon atoms into a chamber simultaneously where said chamber contains said substrate and a hafnium target.

Matsuo and Yu are analogous art because they are from the same field of endeavor and a process of depositing HfN on the substrate.

At the tome of invention it would have been obvious to a person of ordinary skill in the art using a process to deposit HfN with flowing Nitrogen and Argon atoms into chamber because of utilizing for its material characterization **(page 230 column 2 lines 11-12)**.

18. Pertaining claim 38, Matsuo fails to teach adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one.

Yu discloses expressly the method according to Claim 36 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one **(Page 230 column 2 lines 15-17 & 29-32)**.

Matsuo and Yu are analogous art because they are from the same filed of endeavor and the name of a process of depositing HfN with flowing Nitrogen and Argon gases.

At the time of invention it would have been obvious to a person of ordinary skill in the art using the method according to Claim 36 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one because HfN films show stoichiometric composition (Hf: N ~1:1).

19. Pertaining claim 39, Matsuo fails to teach expressly further comprising impurity doping into said hafnium nitride layer to tune the work function of said gate electrode.

Yu discloses expressly further comprising impurity doping into said hafnium nitride layer to tune the work function of said gate electrode (Page 230 column 2 lines 35-38, please note combining Yu's method of impurity doping into Matsuo's tuning the work function of gate electrode).

Matsuo and Yu are analogous art because they are from the same filed of endeavor and the name of a process of tuning the work function of gate electrode

At the time of invention it would have been obvious to a person of ordinary skill in the art combining the Yu's method of impurity doping into the Matsuo's methods of fabrication semiconductor process because of oxidization and conversion into HfO_xN_y (Page column 2 lines 35-37).

Therefore, it would have been obvious to combine a Yu's method into Matsuo methods for the benefit of newly crystalline plane by the HfO_xN_y to obtain the invention as specified in claim.

20. Pertaining claim 43, Matsuo discloses first metal layer comprises hafnium nitride and the second metal layer comprise tantalum nitride. Matsuo fails to teach first metal layer comprises tungsten or tantalum nitride and wherein said second metal layer comprises hafnium nitride.

Changes in sequence or process steps are merely nothing more than a prima facie obvious in the absence of new or unexpected results.

See Ex parte Rubin, 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d

690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Pertaining claims 44 & 49, Matsuo fails to teach expressly deposing of hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously where said chamber contains said substrate and a hafnium target.

Yu discloses deposing of Hafnium nitride (HfN) layer comprise flowing Nitrogen and Argon atoms into a chamber simultaneously where said chamber contains said substrate and a hafnium target.

Matsuo and Yu are analogous art because they are from the same field of endeavor and a process of depositing HfN on the substrate.

At the tome of invention it would have been obvious to a person of ordinary skill in the art using a process to deposit HfN with flowing Nitrogen and Argon atoms into chamber because of utilizing for its material characterization **(page 230 column 2 lines 11-12)**.

21. Pertaining claims 45 & 50, Matsuo fails to teach the method according to Claims 44 & 49 further comprising adjusting the flow rate to adjust the work-function of said gate electrodes wherein the atomic ratio of nitrogen to hafnium remains greater than or equal to one.

Yu discloses expressly the method according to Claims 44 & 49 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one **(Page 230 column 2 lines 15-17 & 29-32)**.

Matsuo and Yu are analogous art because they are from the same filed of endeavor and the name of a process of depositing HfN with flowing Nitrogen and Argon gases.

At the time of invention it would have been obvious to a person of ordinary skill in the art using the method, further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrode wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one because HfN films show stoichiometric composition (Hf: N ~1:1).

22. Pertaining claims 46 & 51, Matsuo fails to teach the method according to Claims 44 & 49further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

Yu discloses expressly further comprising impurity doping into said hafnium nitride layer to tune the work function of said gate electrode (Page 230 column 2 lines 35-38, please note combining Yu's method of impurity doping into Matsuo's tuning the work function of gate electrode).

Matsuo and Yu are analogous art because they are from the same filed of endeavor and the name of a process of tuning the work function of gate electrode

At the time of invention it would have been obvious to a person of ordinary skill in the art combining the Yu's method of impurity doping into the Matsuo's methods of fabrication semiconductor process because of oxidization and conversion into HfO_xN_y (Page column 2 lines 35-37).

Therefore, it would have been obvious to combine a Yu's method into Matsuo methods for the benefit of newly crystalline plane by the HfO_xN_y to obtain the invention as specified in claim.

23. Pertaining claims 47 & 52, Matsuo discloses the method according to Claims 44 & 49 further comprising thermal treatment Matsuo fails to teach temperature range and time at about 1000 ^{o}C for about 20 seconds.

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. *See In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodru* ; 919 f 2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizake*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Su C. Kim
11/09/2005

W. DAVID COLEMAN
PRIMARY EXAMINER